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10/790,203	03/02/2004	Toshio Miyazawa	501.40202CX1	1027

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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
SHAPIRO, LEONID	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/790,203	Applicant(s) MIYAZAWA ET AL.	
	Examiner Leonid Shapiro	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6,8-12,14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. (US Patent No. 5,712,652) in view of Hideo (JP 58023091).

As to claim 1, Sato et al. teaches an active matrix type display device (See Fig.19, item 904, Col. 1, Lines 34-50) comprising:

a substrate (See Fig.19, item 906, Col. 1, Lines 34-40);

a scanning line formed on the substrate (See Fig.10, items 2-1,2-2, Col. 15, Lines 23-25);

a video signal line formed on the substrate (See Fig.10, items 2-1,2-2, Col. 15, Lines 31-35);

a transistor connected to the scanning signal line and the video signal line (See Fig.10, item 21, Col. 15, Lines 36-42);

a first inverter circuit connected to the transistor and formed on the substrate (See Fig.10, items 22-23, Col. 15, Lines 36-50);

a second inverter circuit connected to the first inverter circuit and formed on the substrate (See Fig.10, items 24-25, Col. 15, Lines 36-50);

a third inverter circuit connected to the second inverter and formed on the

substrate (See Fig.10, items 28, Col. 15, Lines 50-60);

a pixel electrode connected to the third inverter circuit (See Fig.10, items 3, 13, 22-23, Col. 15, Lines 50-60).

Sato et al. does not disclose a pair of AC power supply lines formed on the substrate, wherein the first inverter circuit and the second inverter circuit are supplied with a pair of AC voltages from the AC power supply lines.

Hideo teaches a pair of AC power supply lines formed on the substrate, wherein the first inverter circuit and the second inverter circuit are supplied with a pair of AC voltages from the AC power supply lines (See Fig. 9. items 22-23, page 9, Lines 3-19).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Hideo into Sato et al. system in order to reduce power consumption (See page 10, Lines 1-6 in the Hideo reference).

As to claim 8, Sato et al. teaches an active matrix type display device (See Fig.19, item 904, Col. 1, Lines 34-50) comprising:

a substrate (See Fig.19, item 906, Col. 1, Lines 34-40);

a scanning line formed on the substrate (See Fig.10, items 2-1,2-2, Col. 15, Lines 23-25);

a video signal line formed on the substrate (See Fig.10, items 2-1,2-2, Col. 15, Lines 31-35);

a transistor connected to the scanning signal line and the video signal line (See Fig.10, item 21, Col. 15, Lines 36-42);

a memory circuit connected to the transistor and formed on the substrate (See Fig.10, items 24-25, Col. 15, Lines 36-50);

a pixel electrode connected to the memory circuit (See Fig.10, items 3, 13, 22-23, Col. 15, Lines 50-60).

Sato et al. does not disclose a pair of AC power supply lines formed on the substrate, wherein the memory circuit is supplied with a pair of AC voltages from the AC power supply lines.

Hideo teaches a pair of AC power supply lines formed on the substrate, wherein the memory circuit is supplied with a pair of AC voltages from the AC power supply lines (See Fig. 9. items 22-23, page 9, Lines 3-19).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Hideo into Sato et al. system in order to reduce power consumption (See page 10, Lines 1-6 in the Hideo reference).

As to claim 14, Sato et al. teaches an active matrix type display device (See Fig.19, item 904, Col. 1, Lines 34-50) comprising:

a substrate (See Fig.19, item 906, Col. 1, Lines 34-40);

a scanning line formed on the substrate (See Fig.10, items 2-1,2-2, Col. 15, Lines 23-25);

a video signal line formed on the substrate (See Fig.10, items 2-1,2-2, Col. 15, Lines 31-35);

a transistor connected to the scanning signal line and the video signal line (See Fig.10, item 21, Col. 15, Lines 36-42);

a memory circuit connected to the transistor and formed on the substrate (See Fig.10, items 24-25, Col. 15, Lines 36-50);

a pixel electrode connected to the memory circuit (See Fig.10, items 3, 13, 22-23, Col. 15, Lines 50-60);

wherein the transistor, the memory circuit, and a pixel electrode are connected in series (See Fig. 10, items 3,13,21-28).

Sato et al. does not disclose a pair of AC power supply lines formed on the substrate, wherein the memory circuit is supplied with a pair of AC voltages from the AC power supply lines.

Hideo teaches a pair of AC power supply lines formed on the substrate, wherein the memory circuit is supplied with a pair of AC voltages from the AC power supply lines (See Fig. 9. items 22-23, page 9, Lines 3-19).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Hideo into Sato et al. system in order to reduce power consumption (See page 10, Lines 1-6 in the Hideo reference).

As to claims 2,11,18 Sato et al. teaches output of the second inverter circuit is connected to an input of the first inverter circuit or are connected in series (See Fig.10, items 22-25).

As to claims 3,9-10,16-17 Hideo teaches AC voltage applied on one line of the pair of AC power supply lines is complementary to an AC voltage applied on the other line of the pair of AC power supply lines (See Figs. 7-9, items 16-18, pages 7-8).

As to claim 4, Sato et al. teaches a fixed voltage line connected to the third inverter circuit (See Fig.10, items, 26-2, 28) and Hideo teaches a pair of AC power supply lines (See Fig. 9, items 22-23).

As to claim 5, Sato et al. teaches wherein the transistor, the memory circuit, and a pixel electrode are connected in series (See Fig. 10, items 3,13,21-28).

As to claims 6,12,19 Sato et al. teaches LCD device (see Col. 1, Lines4-9).

As to claim 15 Sato et al. teaches the transistor and the pixel electrode are not connected directly (See Fig.10, items 3,21).

3. Claims 7,13,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al, Hideo as applied to claims 1,8,14 above, and further in view of Troutman (Pub. No.: US 2001/0043173 A1).

Sato et al, Hideo do not disclose electroluminescence display device.

Troutman teaches electroluminescence display device (See paragraph 0004).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Troutman into Hideo into Sato et al. system.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS
01.05.07

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600